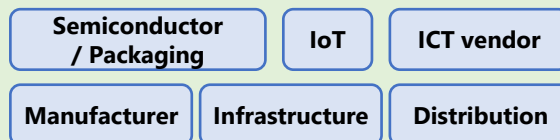


Countermeasure Technologies against Hardware Trojan

NAIST•Kobe Univ.•Tohoku Univ.•YNU
•Electronic Commerce Security Technology Research Association

This technology detects hardware Trojans mounted on PCB during the manufacturing process of the device and after it is shipped. It then ensures the hardware security as the root of trust.

Application Area



Technical Features

Hardware Trojan detection methods

We are developing detection methods of hardware Trojan mounted on the PCB board after the manufacturing process and fabrication. Based on this, we will secure hardware security as the root of trust.

Formal verification methods for hardware Trojan-free IC design

We are integrating hardware logical description verification methods for IP cores and formal verification used for software security. Based on this, we will build fundamental theories that guarantee hardware Trojan-free IC design.

Effects•Use Case•Technical Details

Effects

Supply chain risk control: Detection of malicious attempts through chip design analysis and continuous observation of system operation.

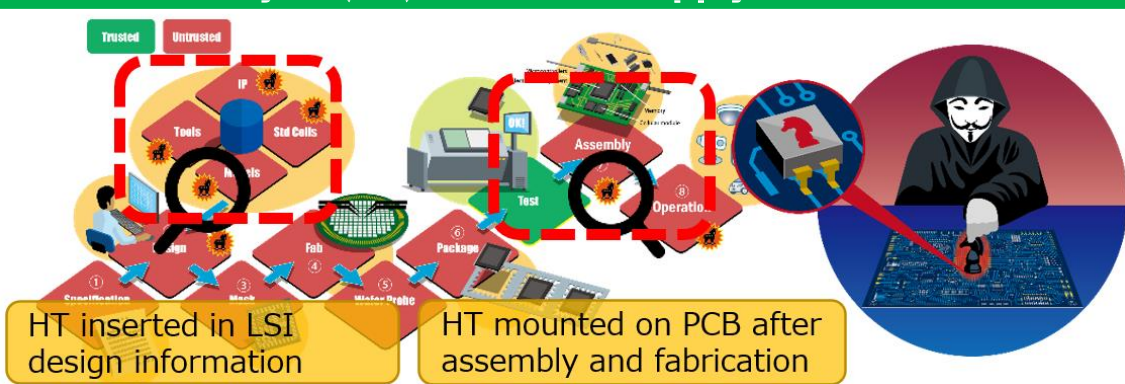
Use Case

By applying this technology to devices equipped with SCU, it is possible to gain resistance to hardware Trojan threats at the board level.

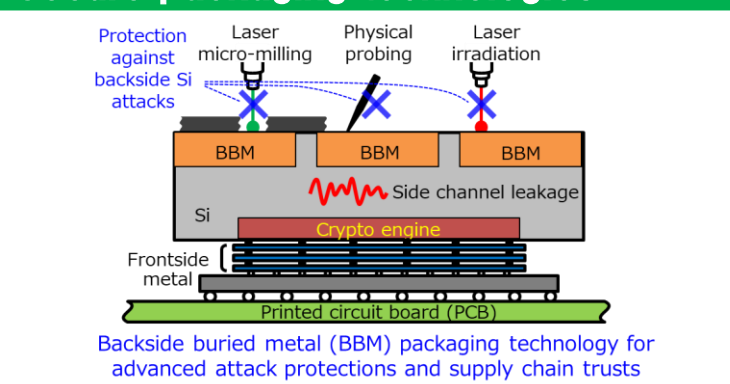
Technical Details

Ensures the security of hardware, which is the basis of trust, by detecting and eliminating malicious functions that may be embedded in hardware during the development, manufacturing, and shipping processes of SCU-equipped devices.

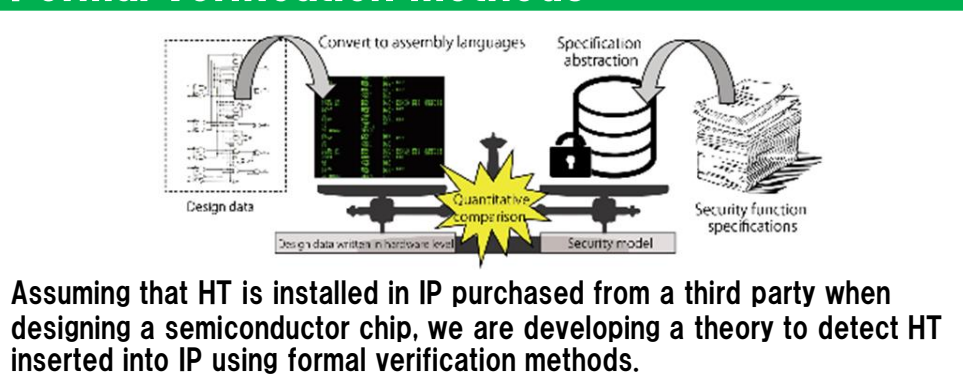
Hardware Trojan (HT) threats in supply chains



Secure packaging technologies

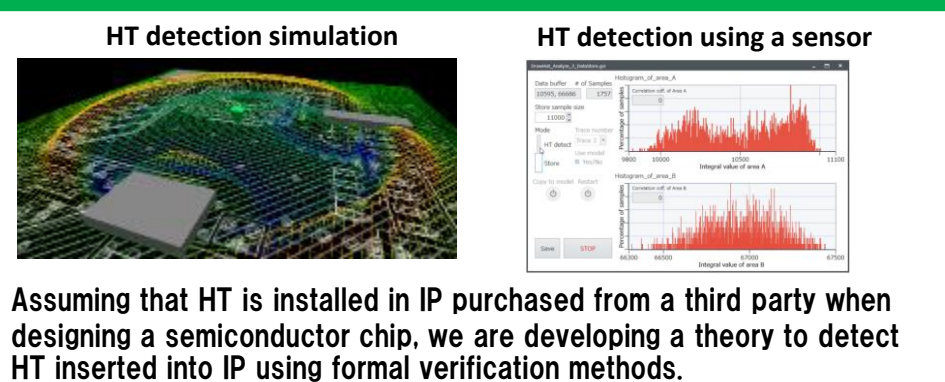


Formal verification methods



Assuming that HT is installed in IP purchased from a third party when designing a semiconductor chip, we are developing a theory to detect HT inserted into IP using formal verification methods.

Electrical detection methods



Assuming that HT is installed in IP purchased from a third party when designing a semiconductor chip, we are developing a theory to detect HT inserted into IP using formal verification methods.