Topological AFRAM Development (Topologic Inc.)



City	Year of Establishment	Founder
Bunkyo-ku, Tokyo	2021	Taiki Sato

Partner VC	Latest round of Fundraising	Valuation
SBI Investment Co., Ltd.	Series A	JPY 100 million

O Business Plan

Develop power-saving magnetic memory technology. By utilizing the characteristics of topological antiferromagnetic materials, this memory technology reduces the energy of spin flips required to write information to 1/1000 of that required for magnetic memory, thereby reducing the power consumption of magnetic memory. This technology will replace DRAM technology commonly used in data centers, and aims to reduce greenhouse gas emissions through power savings.

Research Outline

In this study, we will verify the basic operation of TL-RAM with a 1-million-bit memory array. In the STS phase, we will first focus on the MTJ fabrication process, where (I) develop and optimize a process to reduce the MTJ device short-circuit failure ratio of 50% or less. In executing this development, integrated manufacturing at the foundry will greatly accelerate development and enable early optimization. Second, (II) design and implement a high-efficiency readout circuit. This will achieve a readout yield of 80% or higher. Third, (III) improve the characteristics of MTJ, the essential part of memory cells, with regard to write power, which is the key to low-power operation. Based on the results of this research and development, we aim to start demonstration testing for model verification in collaboration with key customers.

Business Area/Field	Research Period	Research Grant Amount	International collaborative technology demonstration
Energy & Infrastructure	STS 2025-2026FY	JPY 267 million	-

Contact Information:

tel: 81-03-5990-9509 e-mail: info@topologic.jp

Website: https://www.topologic.jp/